IN THE CLAIMS:

Please amend the pending claims as follows:

1. (Previously Presented) A method of filtering over-sampled data comprising:

a. receiving a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits;

b. detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and

c. outputting the received word with the sample bit having said one logic value inverted.

2. (Previously Presented) A method of filtering over-sampled data comprising:

a. receiving a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits;

b. detecting a sample bit having one logic value and, on either side of it, bits having an opposite logic value wherein said detecting comprises:

b1. exclusively ORing each sample bit in said word separately with each bit on either side of the sample bit; and

b2. ANDing the results of said exclusive ORing; and

c. outputting the received word with the sample bit having said one logic value inverted.

3. (Previously Presented) The method of claim 2 and further including providing a history bit to supply a bit to be exclusively ORed with the most significant bit of said word.

4. (Previously Presented) The method according to claim 3 wherein a plurality of words in succession are received, with the operations a, b, and c of claim 2 performed for each word, and further including saving the least significant bit of a last previous word received as the history bit for the next word received.

5. (Original) The method according to claim 4 comprising receiving words until the end of a packet is reached.

6. (Previously Presented) The method of claim 2 wherein said outputting comprises outputting each of said sample bits uninverted if the result of said ANDing is one logic level and inverted if the result is the other logic level.

7. (Previously Presented) The method according to claim 1 further comprising over-sampling said data and receiving said word from at least one over-sampler.

8. (Original) The method according to claim 7 and further comprising selecting a word to be received from between two over-samplers.

9. (Original) The method according to claim 1 wherein said over-sampled data is USB 2.0 data.

10. (Previously Presented) Apparatus for filtering over-sampled data comprising:

a. detection logic coupled to receive a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and

b. an output circuit outputting the received word with the sample bit having said one logic value inverted.

11. (Previously Presented) Apparatus for filtering over-sampled data comprising:

a. detection logic coupled to receive a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and on either side of it, bits having an opposite logic value, said detection logic further comprises

a1. a plurality of terminals for receiving said sample bits for each of a plurality of data bits;

a2. a plurality of first two input logic circuits to perform an exclusive OR function, each having its inputs coupled to two adjacent terminals; and

a3. a plurality of second two input logic circuits to perform an AND function, each having as inputs outputs of two adjacent first logic circuits

b. an output circuit outputting the received word with the sample bit having said one logic value inverted.

12. (Original) The apparatus of claim 11 and further including a storage element to store a history bit, an output of said storage element coupled to one of said first logic circuits having as a second input a sample bit which is most significant.

13. (Original) The apparatus of claim 12 wherein said output circuit comprises:

a. a plurality of inverters, one coupled to each terminal; and

b. a plurality of multiplexers, each having a first data input coupled to an output of one of said inverters, an second data input coupled to the corresponding terminal, and a control input coupled to the output of the one of said second logic circuits associated with said terminal and an output.

14. (Original) The apparatus of claim 13 wherein a plurality of words in succession are to be received, said storage element having an input coupled to the least significant sample bit and having a clock input to clock said input to its output prior to receiving a new word.

15. (Original) The apparatus of claim 14 and further comprising an over-sampler to supply said words to said terminals.

16. (Original) The apparatus of claim 15 wherein two over-samplers are provided and further including a selection circuit to select between two over-samplers.

17. (Original) The apparatus of claim 16 wherein said selection circuit is a multiplexer.

18. (Previously Presented) The apparatus of claim 13 wherein said over-sampled data is USB 2.0.

19. (Previously Presented) A computer readable memory containing program instructions that, when executed by a processor, cause the processor to:

a. receive a word of over-sampled data including a plurality sample bits for each of a plurality of data bits;

b. detect a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and

c. output the received word with the sample bit having said one logic value inverted.

20. (Previously Presented) A computer readable memory containing program instructions that, when executed by a processor, cause the processor to:

a. receive a word of over-sampled data including a plurality sample bits for each of a plurality of data bits;

b. detect a sample bit having one logic value and, on either side of it, bits having an opposite logic value

c. exclusively OR each sample bit in said word separately with each of the bits on either side of the sample bit; and

d. AND the results of said exclusive ORing; and

e. output the received word with the sample bit having said one logic value inverted.

21. (Previously Presented) A computer readable memory according to claim 20 wherein said processor is caused to provide a history bit to supply a bit for exclusive ORing with the most significant bit of said word.

22. (Previously Presented) A computer readable memory according to claim 21 wherein said processor is caused to receive a plurality of words in succession, with the operations a.-e. performed for each word and said processor is further caused to save the least significant bit of a last previous word received as the history bit for the next word received.

23. (Original) A computer readable memory according to claim 22 wherein said processor is caused to receive words until the end of a packet is reached.

24. (Original) A computer readable memory according to claim 23 wherein said processor is caused to output said each sample bits uninverted if the result of said ANDing is one logic level and inverted if the result is the other logic level.

25. (Original) A computer readable memory according to claim 21 wherein said over-sampled data is USB 2.0 data.